

### REMARKS

In response to the Office Action mailed March 8, 2006, the Applicants respectfully request reconsideration. To further the prosecution of this Application, the Applicants submit the following remarks and have canceled claims. The claims as now presented are believed to be in allowable condition.

Claims 13 and 15-28 were pending in this Application. By this Amendment, claim 19 has been cancelled and claim 1 amended, in part, to include content of cancelled claim 19. Additionally, claims 21-28 have been canceled. Applicants expressly reserve the right to prosecute at least some of canceled claims 21-28 and similar claims in one or more related Applications. Accordingly, claims 13, 15-18, and 20 are now pending in this Application. Claim 13 is an independent claim.

### Claim Objections

Claim 25 was objected to because of various informalities regarding antecedent basis. Claim 25 has been cancelled. In light of the cancellation of claim 25, the objection is improper.

### Rejections under §103

Claims 13, 15, 18, 20, 21, 24, and 25 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,627,822 to Jackson in view of U.S. Patent No. 6,736,306 to Byun. Claims 16 and 22 was rejected under 35 U.S.C. §103(a) as being unpatentable over Jackson in view of in view of Byun and further in view of U.S. Patent No. 6,600,220 to Barber. Claims 17 and 23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Jackson in view of in view of Byun and further in view of U.S. Patent No. 6,787,920 to Amir. Claims 19, 26, and 27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Jackson in view of in view of Byun and further in view of U.S. Patent No. 6,396,136 to Kalidas. Claim 28 was rejected under 35 U.S.C.

§103(a) as being unpatentable over Jackson in view of in view of Byun, Amir, and Barber.

The Applicants respectfully traverse each of these rejections and request reconsideration. The claims are in allowable condition. In light of the amendment of claim 13 with content of cancelled claim 19, the rejection of claim 19 will be addressed below.

As amended, claim 13 relates to a method for manufacturing an area array package. The method includes coupling a grid array of primary electrical contacts to a coupling surface of a substrate within a central portion defined by the substrate where the grid array of primary electrical contacts is configured to carry at least data signals between the area array package and a circuit board. The primary electrical contacts of the grid array are formed as a plurality of primary solder balls where each primary solder ball of the grid array defines a first diameter. The method further includes coupling a series of secondary electrical contacts to the coupling surface of the substrate within a peripheral area defined by the coupling surface where the series of secondary electrical contacts is configured to carry power signals between the area array package and the circuit board with the series of secondary electrical contacts being separate from the grid array. The series of secondary electrical contacts are formed as a plurality of secondary solder balls where each secondary solder ball of the series defines a second diameter and where the second diameter defined by each of the secondary solder balls is greater than the first diameter defined by each of the primary solder balls. The method also includes, when coupling the series of secondary electrical contacts, coupling the series of secondary electrical contacts to the coupling surface of the substrate, the coupling surface configured to oppose a mounting surface of the circuit board, the substrate having at least one power plane, at least one ground plane, at least one plated through hole in communication with the at least one power plane, and at least

one plated through hole in communication with the ground plane. The substrate also has a contact pad in electrical communication with the at least one plated through hole in communication with the at least one power plane and electrically coupled with a secondary solder ball of the series of secondary electrical contacts. The substrate has a contact pad in electrical communication with the at least one plated through hole in communication with the at least one ground plane and electrically coupled with a secondary solder ball of the series of secondary electrical contacts. The secondary solder ball, contact pad, and the at least one plated through hole in communication with the at least one power plane configured to carry power to the at least one power plane through the coupling surface. The secondary solder ball, contact pad, and the at least one plated through hole in communication with the at least one ground plane configured to carry power from the at least one ground plane through the coupling surface.

Jackson generally relates to an electronic assembly with separate power and signal connectors. In particular, the electronic assembly in Jackson includes a substrate 108, such as a semiconductor chip or a socket to hold a semiconductor chip, having a multiplicity of solder balls 114. Each solder ball 114 can be melted to form a signal connection with corresponding conductive pads of a printed circuit board 101. The electronic assembly also includes a plurality of pins 110 that electrically connect with holes formed in the printed circuit board to form power connections between the substrate and the circuit board.

Byun generally relates to a semiconductor chip package configured to prevent cracks from forming between external connection terminals, such as solder balls and ball pads. In Byun, a board-mounted BGA package 200 includes a chip 110 mounted on a substrate 120 and enhanced pads 170 formed at the outer edges of the bottom surface of the substrate 120. Each of the enhanced pads 170 includes a ball pad 124, at least one dummy pad 174, and a

dummy pattern 172 that connects the ball pad 124 to the dummy pad 174. In Byun, when mounting the BGA package to a board 150 using the enhanced pads 170, solder balls 160 are formed on both the ball pads 124 and the dummy pads 174 of the substrate 120. The solder balls 160 then undergo a solder reflow process to form a connection terminal 162 over an entire area of the enhanced pad.

Kalidas relates to electrical interconnections in a ball grid array (BGA) package. The BGA package of Kalidas includes an interposer circuit, an embodiment of which is shown in Figs. 4a and 4b, that “facilitates routing of signal, power and ground through the use of selective planes and buses with specific boundaries on only two conductor layers, as opposed to four or more layers required with multilayer substrates. Column 4, lines 49-54. With respect to Fig. 4a in Kalidas:

[a] plurality of power and ground contacts on the integrated circuit 400, located in the center of the flip chip are connected to corresponding contact pads on the first conductive surface of the interposer. *Ground contacts 404a made to conductive vias 405 are surrounded by apertures 405a in the otherwise continuous conductive metal power plane 403. The vias 405 provide contact to the ground plane 404 on the second conductor surface.* The broad area of metal corresponding to the center of the chip is one power plane 403. Column 5, lines 8-17 (emphasis added).

Kalidas further describes an embodiment of the interposer circuit with respect to Fig. 7. As shown in Fig. 7, an interposer circuit 703 includes multiple power planes on the first metal layer 703a and a ground plane on the second metal layer 703b. Column 7, lines 61-64. Furthermore in Kalidas:

[t]he BGA package 700 includes a stiffener or base 704 with conductive vias 704c between the external BGA solder ball terminals 705 and contact pads on the upward facing surface 704a. Connection between the base vias 704c and the interposer vias 703c is provided by a plurality of solder bumps 708 on the second surface of the interposer circuit 703b. The ground plane covers the center portion of the second surface of the interposer circuit, and

apertures are provided for vias for signal and power contacts near the perimeter. Column 7, line 65 - column 8, line 8.

As indicated above, claim 19 was rejected under 35 U.S.C. §103(a) as being unpatentable over Jackson in view of in view of Byun and further in view of Kalidas. However claim 13, as amended, is not unpatentable over Jackson in view of in view of Byun and further in view of Kalidas because none of the references, either alone or in combination, teach or suggest all of the elements of the claim.

The Office Action recites on page 9, paragraph 3 that Jackson and Byun “do not specifically teach the method wherein the substrate defines at least one power plane, at least one ground plane, and at least one plated through hole in communication with the at least one power plane and the at least one ground plane, the substrate further comprising a contact pad in electrical communication with the at least one plated through hole and configured to electrically couple with a secondary solder ball.” The Office Action instead relies on Kalidas to supply such a teaching. Kalidas, however, does not cure the deficiencies of either Jackson or Byun. Specifically, Kalidas does not teach or suggest a secondary solder ball, contact pad, and at least one plated through hole in communication with the at least one power plane configured to carry power to the at least one power plane through a coupling surface of the substrate and a secondary solder ball, contact pad, and at least one plated through hole in communication with the at least one ground plane configured to carry power from the at least one ground plane through the coupling surface of the substrate as recited in claim 13.

As indicated above, for the interposer vias of Kalidas, shown in the embodiment in Figs. 4a and 4b, the vias provide contact to the ground plane 404 on the second conductor surface of the interposer and the ground contacts made to the conductive vias are surrounded by apertures in the otherwise continuous

conductive metal power plane. The vias of in the embodiment in Figs. 4a and 4b Kalidas are not in communication with the power plane but are in communication only with the ground plane. As such, Kalidas does not teach or suggest a secondary solder ball, contact pad, and at least one plated through hole in communication with the at least one power plane configured to carry power to the at least one power plane *through a coupling surface of the substrate* and a secondary solder ball, contact pad, and at least one plated through hole in communication with the at least one ground plane configured to carry power from the at least one ground plane *through the coupling surface of the substrate*.

Furthermore, in the embodiment shown in Kalidas' Fig. 7, Kalidas discloses a base 704 having conductive vias 704c between external BGA solder ball terminals 705 and contact pads on the upward facing surface 704a. Solder bumps provide a connection between the base vias 704c and the interposer vias 703c. As described in Kalidas, "[t]he ground plane covers the center portion of the second surface of the interposer circuit, and *apertures are provided for vias for signal and power contacts near the perimeter*. With reference to Fig. 7 and based upon this disclosure, it appears that the interposer vias 703 are used for signal and power planes, as opposed to the ground plane. As such, because the interposer vias 703c are in communication with the signal and power planes and the conductive vias 704c of the base 704 are coupled to the interposer vias 703, the conductive vias of the base 704 are in communication with the power planes of the interposer only and are not in communication with the ground plane. As such, Kalidas does not teach or suggest a secondary solder ball, contact pad, and at least one plated through hole in communication with the at least one power plane configured to carry power to the at least one power plane *through a coupling surface of the substrate* and a secondary solder ball, contact pad, and at least one plated through hole in communication with the at least one ground plane configured to carry power from the at least one ground plane *through the coupling surface of the substrate* as claimed by the Applicants.

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Because none of Jackson, Byun, or Kalidas, teaches or suggests all of the elements of claim 13 and for the reasons stated above, claim 13 patentably distinguishes over the cited prior art, and the rejection of amended claim 13 under 35 U.S.C. §103(a) should be withdrawn. Accordingly, claim 13 is in allowable condition. Because claims 15-18 and 20 depend from and further limit claim 13, claims 15-18, and 20 are in allowable condition for at least the same reasons.

#### Newly Added Claims

Claims 29 has been added and is believed to be in allowable condition. Support for the claim can be found within the Specification, for example, on page 9, line 13 through page 10, line 5. No new matter has been added.

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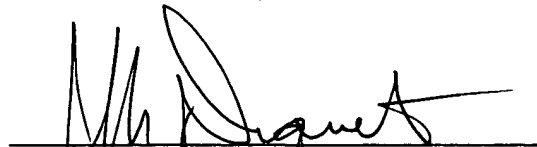
Conclusion

In view of the foregoing remarks, this Application should be in condition for allowance. A Notice to this affect is respectfully requested. If the Examiner believes, after this Response, that the Application is not in condition for allowance, the Examiner is respectfully requested to call the Applicants' Representative at the number below.

The Applicants hereby petition for any extension of time which is required to maintain the pendency of this case. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 50-3661.

If the enclosed papers or fees are considered incomplete, the Patent Office is respectfully requested to contact the undersigned collect at (508) 616-2900, in Westborough, Massachusetts.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Jeffrey J. Duquette", is written over a horizontal line.

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